REMARKS

Prior to an examination of the application on the merits, Applicants respectfully request entry of this preliminary amendment. The specification has been amended. Additionally, claims 1 – 12 have been amended to place the claims in standard format, as well as to correct grammatical and idiomatic errors. The changes to the claims have not been made for any reason related to the patentability of the claims, and have not been made to limit the scope of the claims.

If there are any other fees due in connection with the filing of this paper, please charge the fees to our Deposit Account No. 50-0310. If a fee is required for an extension of time under 37 C.F.R. § 1.136 not accounted for above, such an extension is requested and the fee should also be charged to our Deposit Account.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached pages are captioned "**Version with Markings to Show Changes Made**."

Respectfully submitted,

MORGAN, LEWIS & BOCKIUS LLP

Dated: April 3, 2002

By: S Bhattacharya
Sam Bhattacharya
Reg. No. 48,107

Customer No. 009629
MORGAN, LEWIS & BOCKIUS LLP
1111 Pennsylvania Avenue, N.W.
Washington, D.C. 20004
Telephone: 202-739-3000
Facsimile: 202-739-3001

Version with Marking to Show Changes Made

IN THE ABSTRACT:

The abstract has been replaced with the following rewritten abstract.

ABSTRACT OF THE DISCLOSURE

The present invention relates to a method **of** manufacturing a code address memory (CAM) cell. The present invention uses a dielectric film in which an oxide film and a nitride film between a floating gate and a control gate in a flash memory cell are stacked as a gate insulating film between a semiconductor substrate and a gate in the CAM cell. Therefore, the present invention can reduce the area of a peripheral circuit region and stably secure repaired data since the CAM cell can be stably driven at a low operating voltage and **an** additional boosting circuit is thus not required.

IN THE CLAIMS:

Claims 1 – 12 have been amended as follows.

1. (Amended) A method of manufacturing a code address memory cell, **the method** comprising the steps of:

forming a gate insulating film in which a plurality of oxide films and nitride films are stacked on a semiconductor substrate;

forming a polysilicon film on said gate insulating film;

etching given regions of said polysilicon film and said gate insulating film to form a gate; and

performing **an** impurity ion implantation process to form a source region and a drain region.

2. (Amended) The method **of** manufacturing a code address memory cell [~~as claimed in~~] **according to** claim 1, wherein said gate insulating film is formed [~~of~~] **by stacking** at least two or more layers of **at least one of** said oxide film and said [~~insulating~~] **nitride** film [~~are stacked~~].

3. (Amended) The method **of** manufacturing a code address memory cell [~~as claimed in~~] **according to** claim 1, wherein said gate insulating film [~~is~~] **has a thickness of about** 30 ~ 300Å [~~in thickness~~].

4. (Amended) The method **of** manufacturing a code address memory cell [~~as claimed in~~] **according to** claim 1, wherein said gate insulating film is formed by stacking a first oxide film, a nitride film and a second oxide film.

5. (Amended) The method **of** manufacturing a code address memory cell [~~as claimed in~~] **according to** claim 1, wherein said gate insulating film is formed by stacking a first oxide film, a first nitride film, a second oxide film and a second nitride film.

6. (Amended) The method **of** manufacturing a code address memory cell [~~as claimed in~~] **according to** claim 1, wherein said gate insulating film is formed by stacking a first oxide film, a first nitride film, a second oxide film, a second nitride film and a third oxide film.

7. (Amended) A method of manufacturing a code address memory cell, **the method** comprising the steps of:

forming a device isolation film in a given region on a semiconductor substrate to define an active region and a device isolation region;

defining said active region into a cell region and a peripheral circuit region by a given process;

forming a tunnel oxide film and a first polysilicon film on the entire structure and then patterning said tunnel oxide film and said first polysilicon film so that said tunnel oxide film and said first polysilicon film can only remain in a given region of said cell region, thus defining a floating gate;

forming an insulating film in which [~~said~~] **an** oxide film and [~~said~~] **a** nitride film are stacked on the entire structure to form a second polysilicon film;

patterning said second polysilicon film and said insulating film so that they can remain only in a given region of said cell region and said peripheral circuit region, thus forming a control gate in said cell region **and** a gate in said peripheral circuit region; and

performing an impurity ion implantation process for a given region of said semiconductor substrate to form a source region and a drain region, so that a flash memory cell is formed in said cell region, and a code address memory cell is formed is said peripheral circuit region.

8. (Amended) The method **of** manufacturing a code address memory cell [~~as claimed in~~] **according to** claim 7, wherein said insulating film is formed [~~of~~] **by stacking** at least two or

more layers of **at least one of** said oxide film and said [~~insulating~~] **nitride** film [~~are stacked~~].

9. (Amended) The method **of** manufacturing a code address memory cell [~~as claimed in~~] **according to** claim 7, wherein said insulating film [~~is~~] **has a thickness of about** 30 ~ 300Å [~~in thickness~~].

10. (Amended) The method **of** manufacturing a code address memory cell [~~as claimed in~~] **according to** claim 7, wherein said insulating film is formed by stacking a first oxide film, a nitride film and a second oxide film.

11. (Amended) The method **of** manufacturing a code address memory cell [~~as claimed in~~] **according to** claim 7, wherein said insulating film is formed by stacking a first oxide film, a first nitride film, a second oxide film and a second nitride film.

12. (Amended) The method **of** manufacturing a code address memory cell [~~as claimed in~~] **according to** claim 7, wherein said insulating film is formed by stacking a first oxide film, a first nitride film, a second oxide film, a second nitride film and a third oxide film.